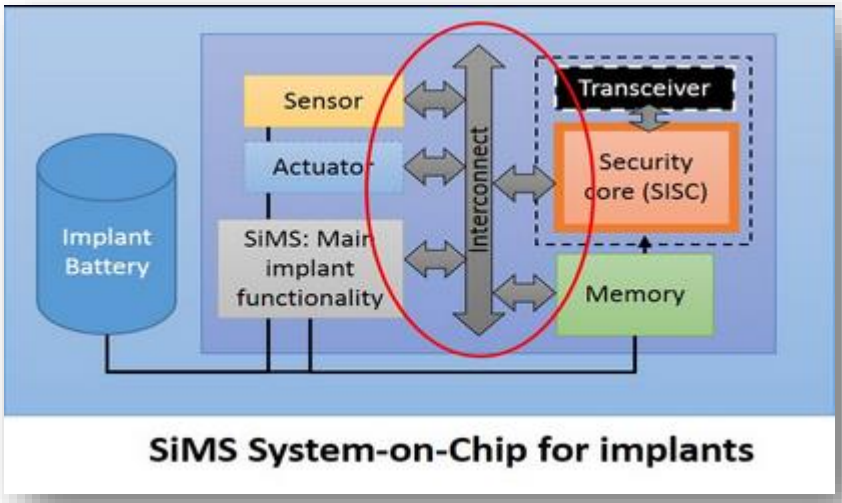
Thesis Topics Related To SINS

This is an indicative list of topics related to the SINS research theme. More topics in this context are often available. Contact us for more details on what is available.

Low-Power, Fault-Tolerant Interconnect for Implant SoCs



Topic:

Implantable Medical Devices (IMDs) are safety-critical devices with ultra-low power constraints, used for the long-term treatment of various medical conditions, such as arrhythmias (using an Implantable Cardioverter Defibrillator (ICD)) or epilepsy (neurostimulator). IMDs employ an ever increasing number of components (sensors, actuators, processors and memory blocks) which communicate with each other in a System-on-Chip (SoC). While the complexity of the SoC is expected to rise, little attention has been given to the interconnect between the various components. This interconnect should respect both the safety constraints (fault tolerance) and low-power constraints imposed by the IMD, while suiting the communication needs of (and number of components in) the SoC. In this topic, the student is expected to design an interconnect suitable for IMDs.

Expected effort:

The student is expected to evaluate various types of interconnects (point-to-point, bus, network-on-chip) considering their fault-tolerance, power consumption and communication capabilities. Based on this evaluation, in which the student will consider various communication patterns based on actual implantable applications available, the student will design and implement an interconnect tailored to IMDs.

Expected outcome:

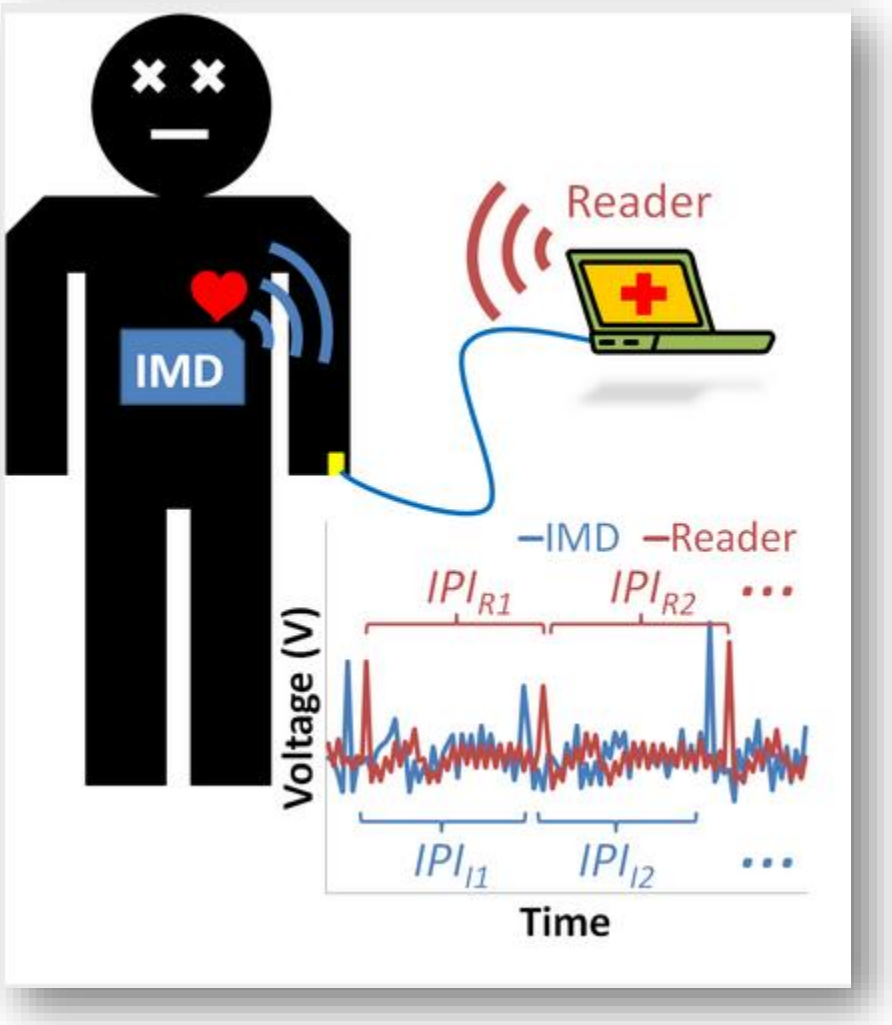
An interconnect design (bus, NoC) tailored to the low-power, high reliability characteristic of implantable devices.

Prerequisites:

The student is expected to have a background in hardware design and experience in VHDL or Verilog. Experience on interconnects and / or systemC is preferred.

Contact: Robert Seepers, Christos Strydis

3. Inter-sensor disparity in heart-beat-based security [up to 2 students]



Topic:

Heart-beat-based security has recently been proposed to facilitate security in mobile-health applications, such as Implantable Medical Devices (IMDs). Previous work has shown that the time between two consecutive heart beats (inter-pulse interval, IPI) contains a significant degree of entropy, allowing it to be used for security-key generation. This key may subsequently be used for facilitating several security aspects, such as entity authentication between two entities which simultaneously sample the same heart beats.

One key concern in heart-beat-based security is the disparity between two cardiac measurements: As each entity will measure a different signal (from a different location and using different equipment), the generated keys will not be identical. This dissimilarity between keys requires tolerance for successful authentication, lowering security in the process. To optimize security, this tolerance should be tailored to the expected disparity between these sensors. However, there currently exist no dataset or model of this disparity, limiting the study of the tolerance required. In this topic, the

student will create a multi-signal database of various cardiac measurements in order to model inter-sensor variability.

Expected effort:

The student(s) will setup a protocol for measuring the cardiac biosignals, considering both a wide range of measurement signals, equipment (ECG, PPG, BP, …), measurement locations (chest, finger, …) and physical states (sitting, lying down, walking, …). Subsequently, the student(s) will carry out the required measurements and store the results in a database. Finally, the student(s) will develop a mathematical model of inter-sensor variability.

Expected outcome:

- A database which contains multi-signal recordings of a wide array of cardiac signals.
- A (uniform) model of inter-sensor variability and evaluating it in the context of security.

Prerequisites:

A background in medicine, biomedical engineering or equivalent, preferably with experience in measuring cardiac signals and / or databases and / or mathematical modeling. This topic may be split into two topics: 1) measuring cardiac signals and storing them in a database; 2) mathematical modeling of inter-sensor disparity and its application in security. Accordingly, the study may be carried out by up to two students.

Contact: Robert Seepers, Christos Strydis

4. SiMS-processor and compiler development [implementation oriented]

Topic:

Implantable Medical Devices (IMDs) are safety-critical devices with ultra-low power constraints, used for the long-term treatment of various medical conditions, such as arrhythmias (using an Implantable Cardioverter Defibrillator (ICD)) or epilepsy (neurostimulator). The SiMS-processor is being developed within Erasmus MC to facilitate the computational power required by many implantable applications, while respecting the tight power constraints pertinent to IMDs [1]. In this topic, the student is tasked a wide range of tasks related to this development, including compiler (bug) fixes and optimizations, standard-library support and setting up a simulator using the Synopsys Processor Designer and Compiler Designer tools.

Expected effort:

The student is expected to first fix known bugs in the compiler and HDL, which serve as a basis to get experience with the Synopsys tools. Afterwards, the student is tasked with using the tools to create a working cycle-accurate simulator, standard-library support in the compiler and compiler and hardware optimizations.

Expected outcome:

A stable, optimized version of the SiMS architecture, including compiler, processor (HDL) and simulator.

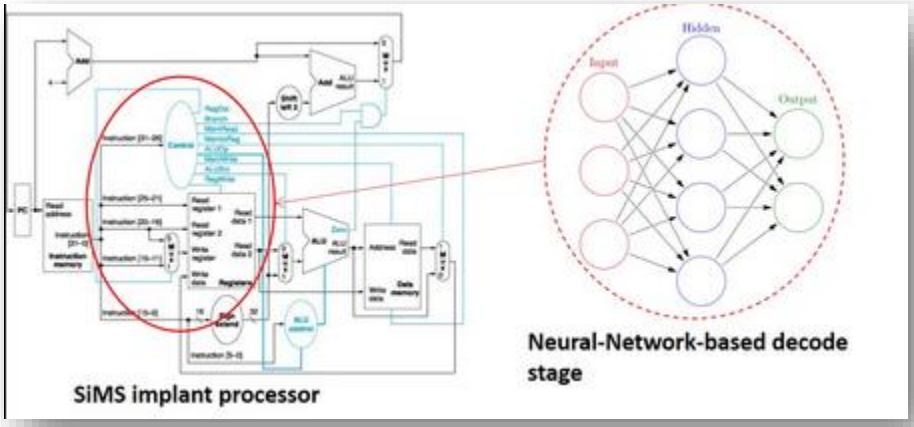
Prerequisites:

The student should have a background in computer engineering or equivalent, having knowledge of processor architectures, hardware design and compilers. This topic is oriented towards implementation.

Contact: Robert Seepers, Christos Strydis

[1] Strydis, Christos, et al. "A system architecture, processor, and communication protocol for secure implants." *ACM Transactions on Architecture and Code Optimization (TACO)* 10.4 (2013): 57.

5. Fault-tolerant decoding for implant processors



Topic:

In the topic of next-generation, smart implantable medical systems (SiMS), a reliable decoder within the SiMS processor is targeted. Atypical decoder may be quite costly in terms of energy and, as all aspects of the core rely on the correct setting of the decode stage, it has to be highly fault-tolerant. As an alternative to conventional fault-tolerant methods (Triple modular redundancy, ECC, etc.), we would like to explore the use of artificial neural networks (ANNs). ANNs are a bio-inspired computing paradigm, where multiple (small) computing elements work together in problem solving by strengthening / weakening the links between them, much like how the human brain works. The advantage of such a paradigm, in terms of reliability, is that the network can potentially recover from a faulty computing element. Previous work on ANNs has shown that these may effectively be used for (fuzzy) ALU-design and memories. This project will explore the applicability of ANNs in a decode stage of a fault-tolerant processor aiming biomedical implants.

Expected effort:

The student is expected to evaluate several ANN schemes and evaluate them (pen and paper or implementation-driven) in terms of overheads (energy, area, …) and robustness (e.g. # nodes which may be removed). Subsequently, the student will implement a traditional decoder using an ANN on the SiMS processor.

Expected outcome:

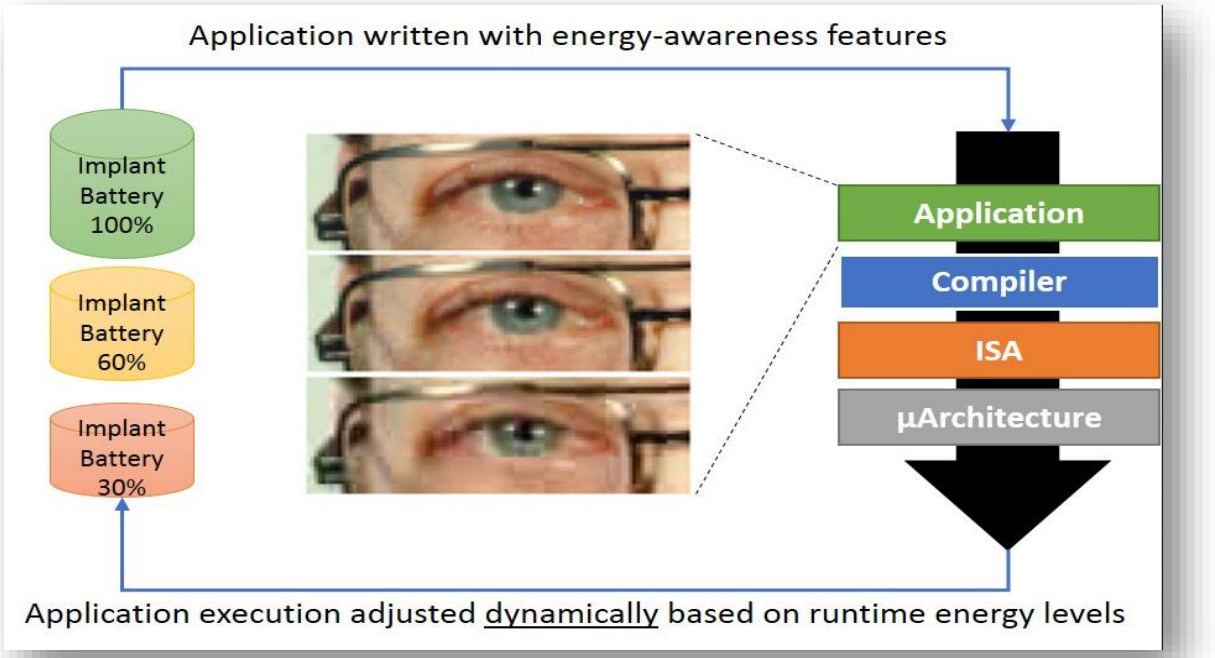
An exploration about the feasibility of using ANNs for a decode stage. This will be the first work on using this paradigm for a reliable decode stage. Due to the novelty of this work it is unknown what the potential overheads and benefits will be.

Prerequisites:

Students with a knowledge of ANNs are preferred.

Contact: Robert Seepers, Christos Strydis

6. Energy-aware Computing for Embedded Devices



Topic:

Modern applications, such as high-definition video, are increasingly power consuming.While there are several techniques available for reducing the power consumption at the processor level (dynamic voltage / frequency scaling, actively powering down of components), it may be beneficial to consider other layers as well (architecture, application). Various applications running on modern embedded systems (such as multimedia) are oblivious to the energy cost they incur on the system battery.The energy consumption of these applications results in a significant drop in battery duration of e.g. a mobile phone. During low-battery mode, it may be beneficial to tune down applications (e.g. reduce the resolution of a video) to allow these applications to be used without endangering battery depletion.

Expected effort:

In this project, the student is expected to develop a programming model which allows a programmer (or: user) to define various profiles as a function of battery usage (energy-aware). For example, in video compression, it may be preferred to decrease the resolution but have a longer lasting battery. Various programming models could readily be adapted, e.g. OmpSs. The student is expected to profile a number of applications (e.g. video, compression, security) and identify code-segments which could be customized.This customization may at first be static (compile-time). Later, the student may propose changes to the ISA and underlying computer architecture to allow for a more dynamic trade-off.

Expected outcome:

A programming model (potentially adapted OmpSs) which allows a programmer to describe different forms / parameters of his or her code, based on the energy levels of a battery. This should subsequently be supported by hardware.

Prerequisites:

Students with knowledge of compiler design (and, secondarily, computer architecture) will be preferred.

Contact: Robert Seepers, Christos Strydis

7. Medium-access control and security in Body-Area Networks using biometrics

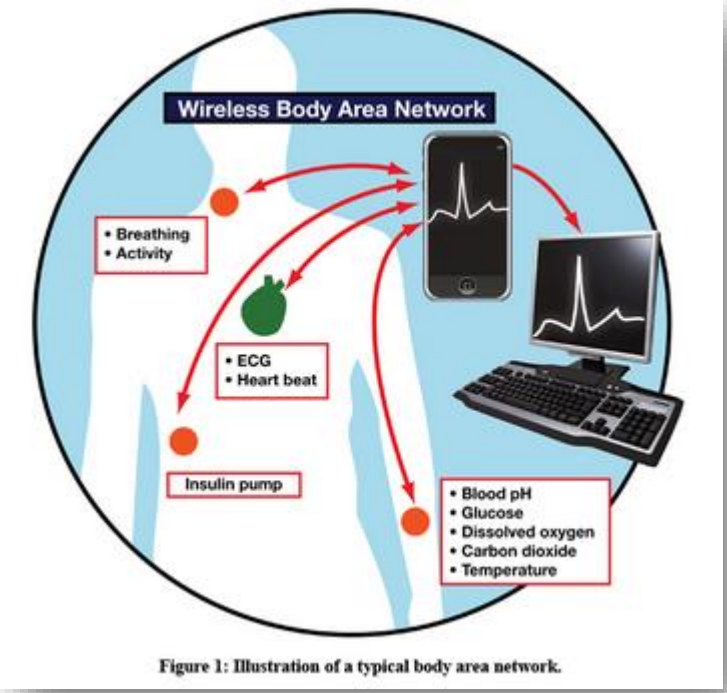


Figure 1: Illustration of a typical body area network.

Topic:

The time interval between heart beats contains a high degree of entropy, while it may be measured remarkably consistent throughout the human body. Accordingly, heart beats are an interesting biometric to be used in Medium-Acces Control (MAC) and security protocols for Body-Area Networks (BANs). Examples of protocols which use heart beats include the Heart-beat-driven MAC (H-MAC) or Heart-to-Heart (H2H) protocols. In this topic, the student is tasked with developing a novel MAC / security protocol which achieves its functionality using biometrics.

Expected effort:

The student is expected to first identify existing MAC and security protocols for BANs which use biometrics (in particular, heart beats). Subsequently, the student will evaluate the most prominent solution(s) (in terms of network lifetime, energy consumption, etc.) and, based on this analysis, will develop a novel MAC / security protocol which uses to achieve its functionality.

Expected outcome:

A security and MAC protocol tailored to BANs, which uses biometrics to achieve of its functionality.

Prerequisites:

The student is expected to have a background in computer science, computer engineering or embedded systems and has basic knowledge of (security) protocols.

Contact: Robert Seepers, Christos Strydis