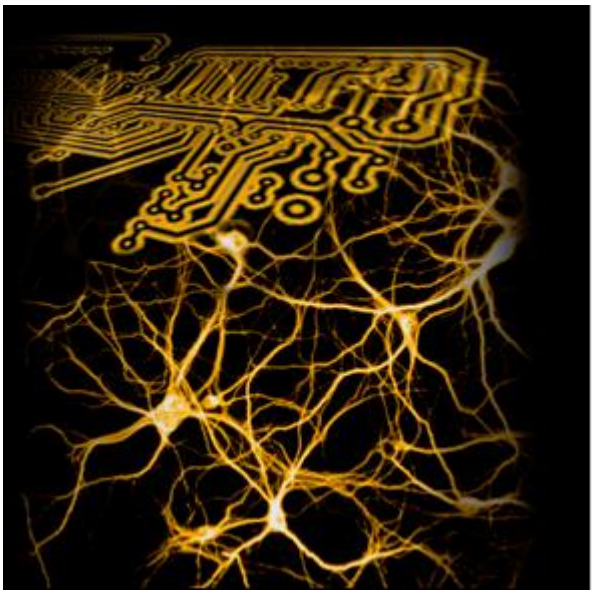
Framework for high-detail and real-time brain simulations (BrainFrame)

Motivation for Brain Emulation

The United States National Academy of Engineers has already classified brain emulation as one of the Grand Engineering Challenges [1]. Brain emulation *in-silico* is a relevant research field for various reasons:



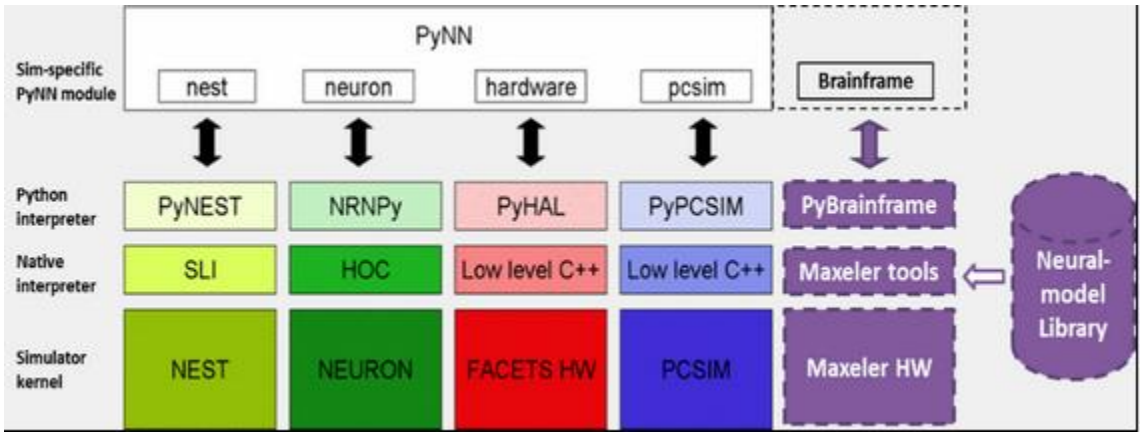
• The immediate benefit of brain emulation is the greater understanding of brain behavior by simulations based on biologically plausible models. Depending on the complexity of the model, it can provide insight on single-cell behavior to network dynamics of whole brain regions without the need for *in-vivo* experiments. This can greatly accelerate brain experimentation and the understanding of the biological mechanisms.

• One important eventual goal of the field is brain rescue. If brain function can be emulated *in-silico* accurately enough and in real time, it can lead to brain prosthetics and implants that can recover brain functionality lost due to health conditions and accidents.

The short term goal of the project is to apply high performance solutions to accelerate and enable large scale accurate brain simulations or enhance data analysis of the experimental data concerning brain research. Thus our activities employ a multitude of HPC node technologies such as FPGAs, Dataflow Computing, GPUs and Many-core processors. The long term goal of this effort is the development of a generic tooling framework for accelerated brain simulations.

The BrainFrame Framework

The eventual goal of the hardware effort is creating a back-end hardware library of designs emulating the full Cerebellum system, based on reconfigurable (DFEs in this case) platforms, as a practical simulation solution for real-time neuro-scientific experiments. This backend will be combined with a PyNN front-end to implement the **BrainFrame** tool-flow. PyNN, a Python-based, simulator-independent language for specification of brain models, is a widely known and used framework by computational neuroscientists. PyNN is capable of achieving high-speed simulation and it already offers a common interface to popular simulation platforms such as NEURON and NEST as well as newly developing ones that show great future potetial, such as NeuroML.

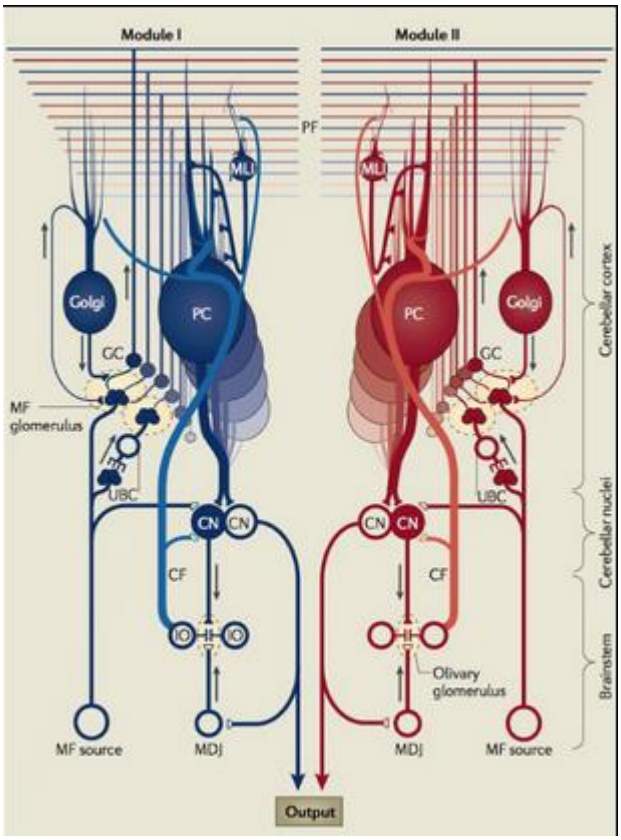


The topics currently worked upon within the BrainFrame research theme are:

- **Acceleration of large-scale brain simulations:** Focused mainly on cerebellar models, exploring the use of various HPC node technologies such as FPGAs, GPUs, dataflow engines and many-core processors (Xeon Phis) for delivering largely scalable, high-speed simulation platforms.
- **Brain rescue and brain-machine interfaces:** Focused mainly on cerebellar models, attempting brain rescue by closing the loop between faulty brain regions and biologically plausible, computational brain models.
- **Powerful, neuroscience-friendly modeling/simulation toolflow**: Exploration and development of both the PyNN front-end and hardware-based back-end for the BrainFrame tooling solution.
- **Improved neuronal recordings and feedback:** Using hardware acceleration for improved signal analysis of single-neuron recording electrodes as well as for enabling closed-loop brain-machine interfaces (i.e. providing brain feedback in relevant brain time scales).

Application Use Case: The Olivocerebellar system

The cerebellum is one of the most complex areas of the brain and plays an important role in motor control. There are also some evidence on its role on cognitive functions.



The cerebellum does not initiate movement but influences the motor control region of the brain in order to guarantee coordination, accurate timing and precision on the body's activities. It also plays an important role in the sensing of rhythm, enabling the understanding of concepts such as music or harmony. Finally, the cerebellum is also imperative for a number of motor-learning skills. Its sensory inputs include the spinal cord and various other brain regions. The cerebellum receives information about peripheral events and central processes through numerous pre-cerebellar systems, which terminate in different layers of the cerebellar cortex, predominantly as climbing and mossy fibers.

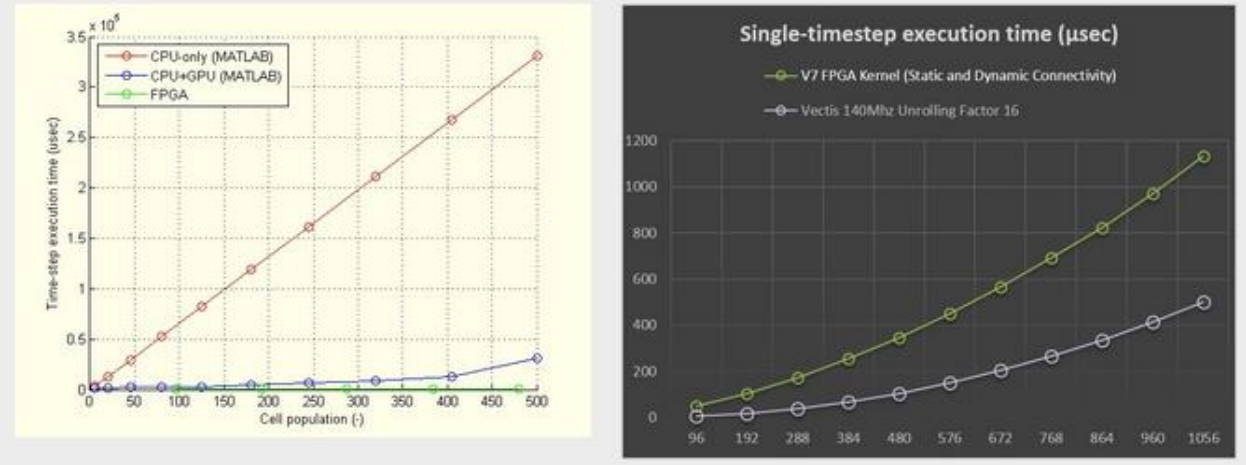
The Olivocerebellar circuitry is a relatively well-charted region of the brain (see figure on the left). Its brain structure is highly repetitive and basically consists of the granule-cell layer (GCL), Purkinje-cell layer (PC), deep-cerebellar-nuclei (DCN), and inferior-olive (IO) nuclei.

The first design effort that we have pursued is the FPGA-based simulation of Inferior-Olive cells, based on an extended-Hodgkin-Huxley (eHH) model of the Inferior-Olive neuron by de Gruijl et al. [2]

This computational model of the cell is largely a dataflow application and requires a few hundred floating-point operations. We have created large networks of Inferior-Olive cells to start approaching realistic brain sizes. The networks need to be massive (>> 10,000) since we aim at modeling millions of neurons in the long run. One good metric of performance is the hardware model's performance compared to "real-time brain computations", that is, the maximum number of cell states that can be computed within the model's simulation time step (in the case of our high-detail Inferior-Olive model: 50 µs).

The FPGA implementation shows speed-ups between x12.5 and x45 compared to a reference, sequential-C implementation and almost x100 compared to the MATLAB implementation typically used in the neuroscientific community to simulate this model. The maximum number of simulated neurons achieved is subject to the complexity of the Inferior-Olive model, the brain real-time constraints (50-µsec neuron update intervals) and the available FPGA area [3].

The same model ported on a Maxeler Vectis Dataflow Engine (DFE) board shows a speed-up between x2 and x7 compared to the FPGA implementation, and is capable of executing a *real-time* network of more than 3 times larger than the FPGA [4]. Indicative performance results on CPU, GPU, FPGA and Maxeler nodes are shown in the comparison charts below.



For related publications see: **BrainFrame publications**

References

[1] National Academy of Engineering (nae.edu), Grand Challenges for Engineering, www.engineeringchallenges.org (2010).

[2] De Gruijl JR, Bazzigaluppi P, de Jeu MTG, De Zeeuw CI, "Climbing Fiber Burst Size and Olivary Sub-threshold Oscillations in a Network Setting", *PLoS Comput Biol 8(12): e1002814 (2012).*

[3] Georgios Smaragdos, Sebastian Isaza, Martijn F. van Eijk, Ioannis Sourdis, and Christos Strydis, "FPGA-based biophysically-meaningful modeling of olivocerebellar neurons", *2014 ACM/SIGDA international symposium on Field-programmable gate arrays* (FPGA '14), ACM, New York, NY, USA, 89-98, 2014.

[4] Georgios Smaragdos, Craig Davies, Christos Strydis, Ioannis Sourdis, Catalin Bogdan Ciobanu, Oskar Mencer, Chris I. De Zeeuw: Real-Time Olivary Neuron Simulations on Dataflow Computing Machines. *ISC 2014: 487-49*